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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,394	12/28/2001	Jum Soo Kim	054216-5016	2075

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SUITE 300  
ALEXANDRIA, VA 22314

EXAMINER
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NGUYEN, KHIEM D

ART UNIT	PAPER NUMBER
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2823

MAIL DATE	DELIVERY MODE
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10/30/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

51

<b>Office Action Summary</b>	<b>Application No.</b> 10/029,394	<b>Applicant(s)</b> KIM ET AL.	
	<b>Examiner</b> Khiem D. Nguyen	<b>Art Unit</b> 2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 24 August 2007.
- 2a) ☐ This action is FINAL.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 7-15 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 7-15 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 March 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicants' submission filed on August 24<sup>th</sup>, 2007 has been entered. A new rejection is made as set forth in this Office Action. Claims (7-15) are pending in the application.

### *Drawings*

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the feature "a device isolation structure in a semiconductor substrate", as recited in claims 7 and 13, line 3, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency.

Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Specification*

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Method of manufacturing code address memory cell by which a stack insulating film of an oxide film and a nitride film used as a dielectric film in a flash memory is used as a gate oxide film.

### *Claim Objections*

4. Claim 9 is objected to because of the following informalities: In dependent claim 9, line 3, replace "□" with --Å--. Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

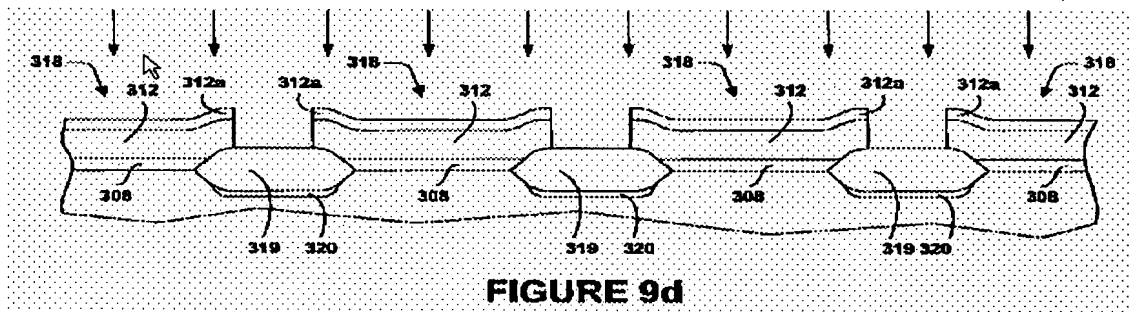
A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

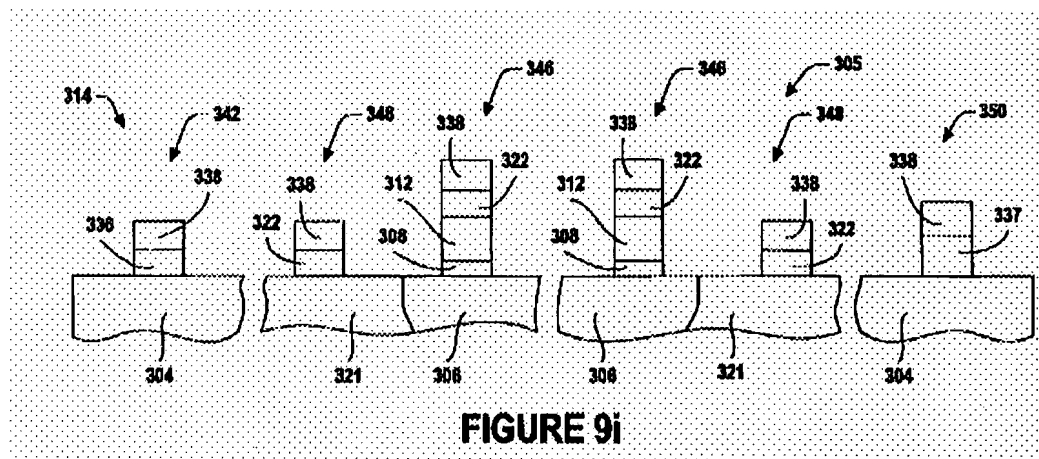
6. Claims 7-10 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Fang (U.S. Patent 6,667,511), of record.

In re claim 7, **Fang** discloses a method of manufacturing a code address memory cell in a peripheral circuit region and a flash memory cell in a cell region, the method comprising:

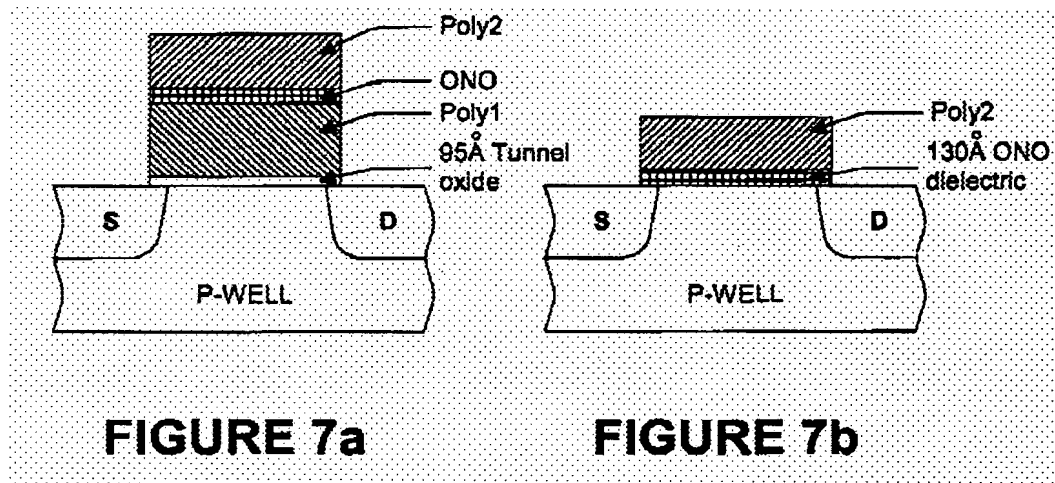
forming a device isolation structure 319 in a semiconductor substrate 304 including the cell region 346 and the peripheral circuit region 348 (see col. 9, lines 16-31 and FIG. 9d, for example);



forming a tunnel oxide layer 308 and a floating gate layer 312 over the cell region 346 (see col. 9, lines 43-56 and FIGS. 7a-b and 9e-i, for example);



forming a dielectric layer 322 and a control gate layer (poly 2) 338 over the floating gate layer (poly1) 312 of the cell region 346 and on the semiconductor substrate 304 of the peripheral circuit region 348 (col. 10, lines 6-65), the dielectric layer 322 including an oxide layer and a nitride layer (ONO) (col. 10, lines 29-38); and forming a source S and a drain D region in the semiconductor substrate 304 by performing an impurity ion implantation process (see FIGS. 7a-b, for example).



In re claim 8, as applied to claim 7 above, **Fang** discloses all claimed limitations including the limitation wherein the dielectric layer 322 is formed by stacking at least two or more layers of at least one of the oxide layer and the nitride layer (oxide-nitride-oxide, ONO layer) (col. 10, lines 29-38).

In re claim 9, as applied to claim 7 above, **Fang** discloses all claimed limitations including the limitation wherein the dielectric layer 322 is formed in thickness of about 130 Å (col. 10, lines 35-36).

In re claim 10, as applied to claim 7 above, **Fang** discloses all claimed limitations including the limitation wherein the dielectric layer 322 is formed by stacking a first

oxide layer (O), a nitride layer (N) and a second oxide layer (O) (ONO) (col. 10, lines 29-38).

In re claim 14, as applied to claim 7 above, **Fang** discloses all claimed limitations including the limitation wherein the floating gate layer **312** and the control gate layer **338** is formed of polysilicon (col. 9, lines 36-42 and col. 10, lines 60-65).

***Claim Rejections - 35 USC § 103***

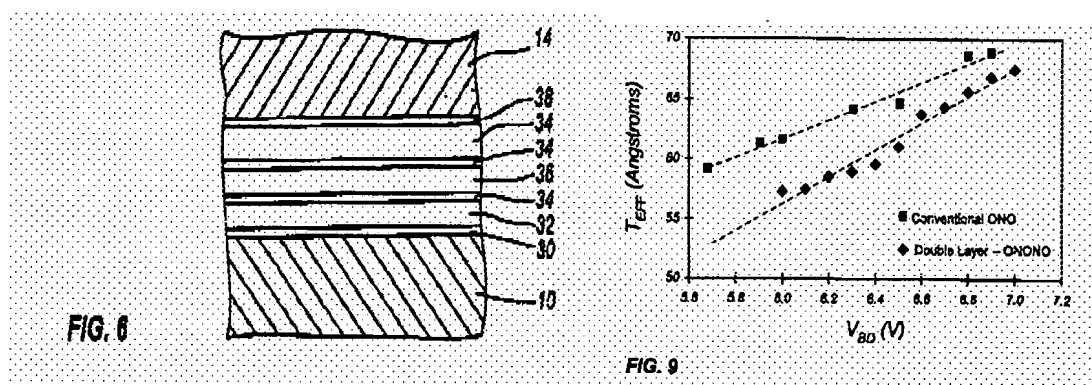
7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fang (U.S. Patent 6,667,511) in view of Sheng et al. (U.S. Patent 5,981,404), both of record.

In re claim 11, as applied to claim 7 Paragraph 5 above, **Fang** discloses a method of manufacturing a code address memory cell in a peripheral circuit region and a flash memory cell in a cell region, the method comprising forming a dielectric layer **322** and a control gate (poly 2) **338** over the floating gate layer (poly1) **312** of the cell region **346** and on the semiconductor substrate **304** of the peripheral circuit region, the dielectric layer **322** including an oxide layer and a nitride layer (oxide-nitride-oxide, ONO) (col. 10, lines 29-38 and FIG. 9i) but does not explicitly disclose that the dielectric layer is formed by stacking a first oxide layer (O), a first nitride layer (N), a second oxide layer (O), and a second nitride layer (N) (ONON).

Sheng et al., however, disclose a insulating structures used in DRAMs or other memory devices such that the dielectric layer is formed by stacking a first oxide layer 30, a first nitride layer 32, a second oxide layer 34, and a second nitride layer 36 (ONON) between the lower doped polysilicon electrode 10 and the upper doped polysilicon electrode 14 (col. 7, lines 41-65 and FIGS. 6 and 9).



As Sheng et al. disclose, one of ordinary skill in the art would have been motivated to provide a dielectric layer formed by stacking a first oxide layer, a first nitride layer, a second oxide layer, and a second nitride layer (ONON) in order to significantly reduced number of defect structures that extend directly through most or all of the dielectric layer (see col. 4, lines 58-61 of Sheng et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant(s) claimed invention was made to modify Fang reference with the dielectric layer formed by stacking a first oxide layer, a first nitride layer, a second oxide layer, and a second nitride layer (ONON) as taught by Sheng et al. in order to significantly reduced number of defect structures that extend directly through most or all of the dielectric layer (see col. 4, lines 58-61 of Sheng et al.).

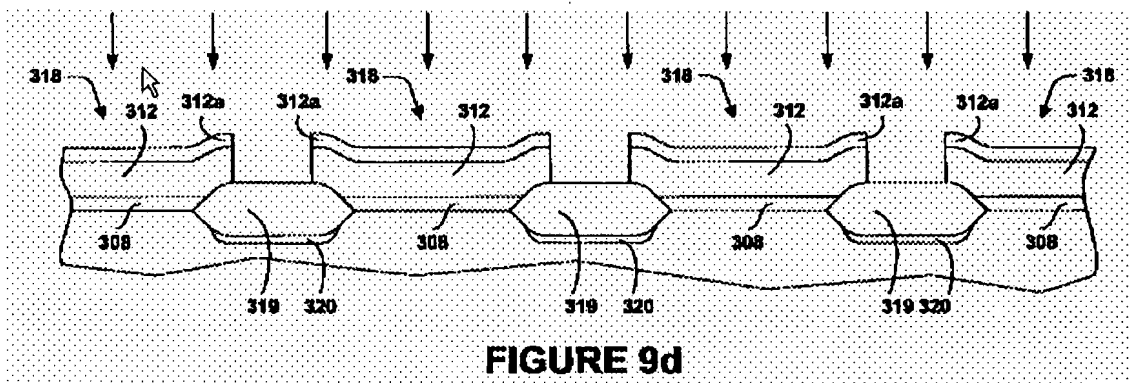


In re claim 12, as applied to claim 7 above, **Fang** in view of **Sheng et al.** discloses all claimed limitations including the limitation wherein the dielectric layer is formed by stacking a first oxide layer 30, a first nitride layer 32, a second oxide layer 34, a second nitride layer 36, and a third oxide layer 34 (ONONO) (see col. 7, lines 41-65 and FIGS. 6 and 9 of Sheng et al.).

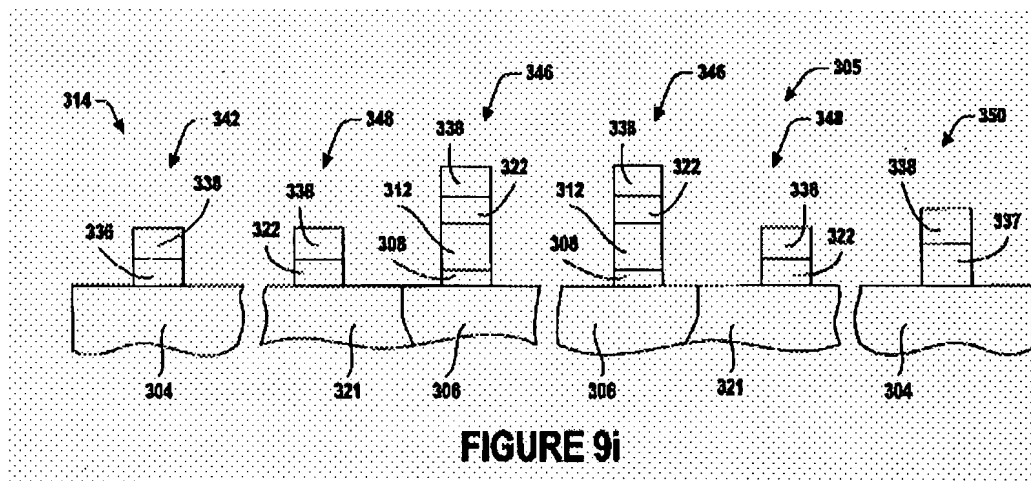
9. Claims 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fang (U.S. Patent 6,667,511) in view of Sheng et al. (U.S. Patent 5,981,404), both of record.

In re claim 13, **Fang** discloses a method of manufacturing a code address memory cell in a peripheral circuit region and a flash memory cell in a cell region, the method comprising:

forming a device isolation structure 319 in a semiconductor substrate 304 including the cell region 346 and the peripheral circuit region 348 (see col. 9, lines 16-31 and FIG. 9d, for example);

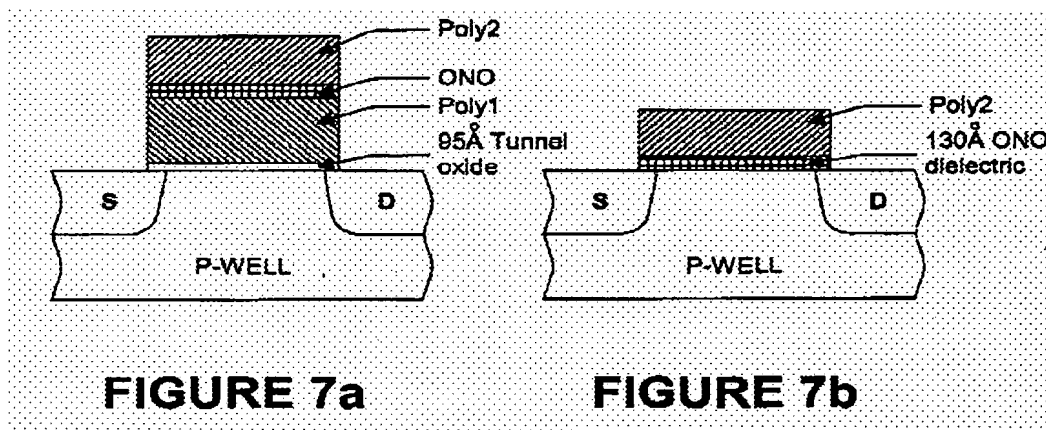


forming a tunnel oxide layer 308 and a floating gate layer 312 over the cell region 346 (see col. 9, lines 43-56 and FIGS. 7a-b and 9e-i, for example);



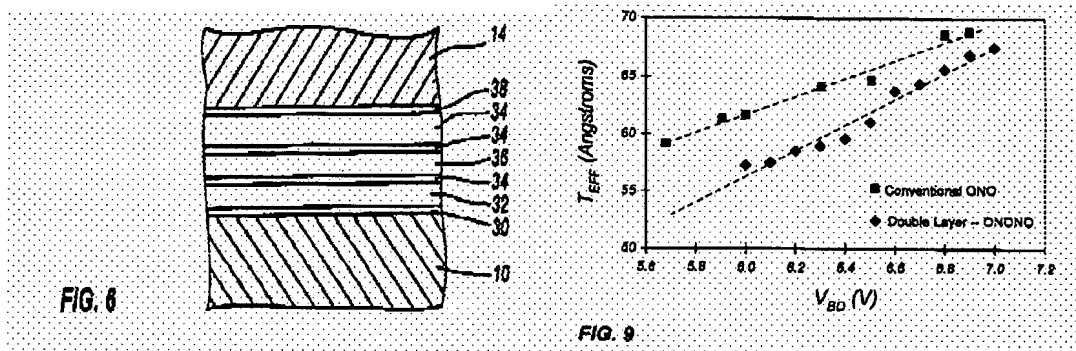
forming a dielectric layer 322 and a control gate (poly 2) 338 over the floating gate layer (poly1) 312 of the cell region 346 and on the semiconductor substrate 304 of the peripheral region 348 (col. 10, lines 6-65), the dielectric layer 322 including an oxide layer, a nitride layer, and an oxide layer (ONO) (col. 10, lines 29-38); and

forming a source S and a drain D region in the semiconductor substrate 304 by performing an impurity ion implantation process (see FIGS. 7a-b, for example).



**Fang** discloses forming a dielectric layer **322** and a control gate (poly 2) **338** over the floating gate layer (poly1) **312** of the cell region **346** and on the semiconductor substrate **304** of the peripheral region **348**, the dielectric layer **322** including an oxide layer, a nitride layer, and an oxide layer (oxide-nitride-oxide, ONO) (col. 10, lines 29-38 and FIG. 9i) but does not explicitly disclose that the dielectric layer including a first oxide layer (O), a first nitride layer (N), a second oxide layer (O), a second nitride layer (N) and a third oxide layer (O) (ONONO).

**Sheng et al.**, however, disclose a insulating structures used in DRAMs or other memory devices such that the dielectric layer is formed by stacking a first oxide layer **30**, a first nitride layer **32**, a second oxide layer **34**, a second nitride layer **36**, and a third oxide layer **34** (ONONO) between the lower doped polysilicon electrode **10** and the upper doped polysilicon electrode **14** (col. 7, lines 41-65 and FIGS. 6 and 9).



As **Sheng et al.** disclose, one of ordinary skill in the art would have been motivated to provide a dielectric layer formed by stacking a first oxide layer, a first nitride layer, a second oxide layer, a second nitride layer, and a third oxide layer (ONONO) in order to significantly reduced number of defect structures that extend directly through most or all of the dielectric layer (see col. 4, lines 58-61 of Sheng et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant(s) claimed invention was made to modify Fang reference with the dielectric layer formed by stacking a first oxide layer, a first nitride layer, a second oxide layer, a second nitride layer, and a third oxide layer (ONONO) as taught by Sheng et al. in order to significantly reduced number of defect structures that extend directly through most or all of the dielectric layer (see col. 4, lines 58-61 of Sheng et al.).

In re claim 15, as applied to claim 13 above, Fang in view of Sheng et al. disclose all claimed limitations including the limitation wherein the floating gate layer 312 and the control gate layer 338 is formed of polysilicon (see col. 9, lines 36-42 and col. 10, lines 60-65 of Fang).

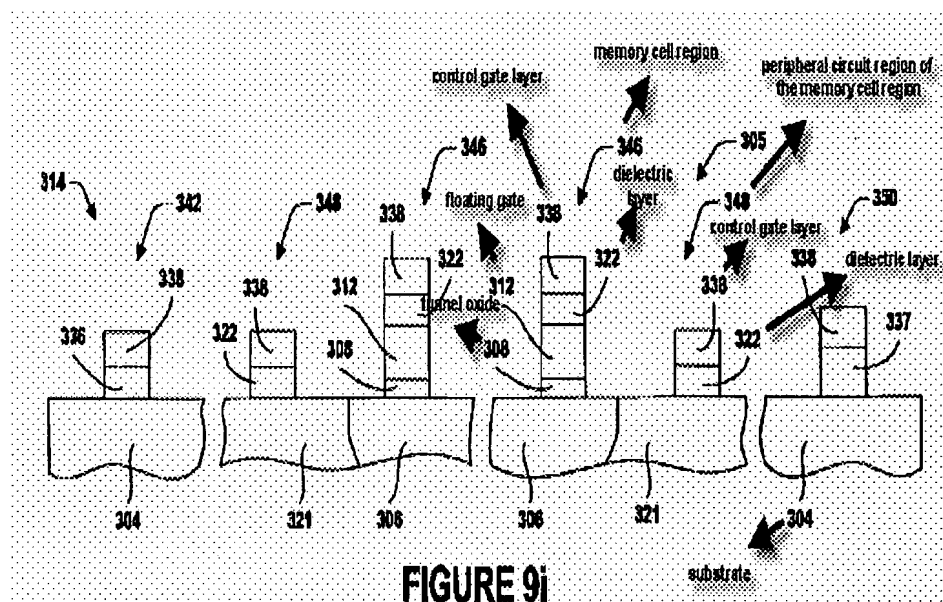
***Response to Applicants' Amendment and Argument***

10. There is no argument presented by the Applicants in the Preliminary Amendment filed on August 24<sup>th</sup>, 2007 (see the Remarks in Page 5 of the August 24<sup>th</sup>, response).
11. Examiner hereby address the argument presented by the Applicants in the Amendment and Response Under 37 CFR § 1.116 filed on August 07<sup>th</sup>, 2007.

Applicants contend that in the claimed invention, the dielectric layer is formed between the control gate and the semiconductor substrate and that the reference, Fang (U.S. Patent 6,667,511), herein known as Fang fails to disclose the dielectric layer. Applicants further contend that Fang shows that a thin gate oxide 336 is formed between a poly2 gate 338 and a substrate 304 in the low voltage peripheral transistor 342, and that a thick gate oxide 337 is formed between the poly2 gate 338 and the substrate 304 in the

In response to Applicants' contention that Fang does not teach or suggest forming a dielectric layer and a control gate layer over the floating gate layer of the cell region and on the semiconductor substrate of the peripheral circuit region, Examiner respectfully disagrees.

Applicants' attention is respectfully directed to (col. 10, lines 29-65 and FIGS. 7a- b and 9e-i, for example) where Fang discloses forming a dielectric layer **322** and a control gate layer **338** over the floating gate layer **312** of the cell region **346** and on the semiconductor substrate **304** of the peripheral circuit region **348** (see illustration of a FIG. 9i below, for example).



Examiner respectfully submits that region 348 is the peripheral circuit region of the memory cell region 346. Therefore, Fang, as illustrated in FIG. 9i, clearly shows that

the dielectric layer **322** and the control gate layer **338** formed over the floating gate layer **312** of the cell region **346** and on the semiconductor substrate **304** of the peripheral circuit region **348**.

In view of above, it is region **348** that the examiner relies upon for the peripheral circuit region of the memory cell region **346** and not the regions **342** or **350** as contended by the Applicants.

For this reason, examiner holds the rejection proper.

***Conclusion***

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Khiem D. Nguyen/  
Examiner, Art Unit 2823

/KN/  
October 26, 2007